Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. OE**
2. **1D**
3. **2D**
4. **3D**
5. **4D**
6. **5D**
7. **6D**
8. **7D**
9. **8D**
10. **GND**
11. **CLK**
12. **8Q**
13. **7Q**
14. **6Q**
15. **5Q**
16. **4Q**
17. **3Q**
18. **2Q**
19. **1Q**
20. **VCC**

**.057”**

**12 11 10 10 9**

**13**

**14**

**15**

**16**

**17**

**18**

**8**

**7**

**6**

**5**

**4**

**3**

**19 20 20 1 2**

**ACT574**

**MASK**

**REF**

**.065”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” x .004” min.**

**Backside Potential: VCC or Float**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .057” X .065” DATE: 7/10/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54ACT574**

**DG 10.1.2**

#### Rev B, 7/19/02